We claim:

1. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$R \cdot C \cdot f < 1$$

where

C = the gate capacitance (F) of said MOS transistor,

R = the resistance (Ω) of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency (Hz) of said predetermined clock, and

$f \geqq 500$ MHz.

2. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region, said gate electrode being electrically connected to said body portion; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said method comprising the steps of:

(a) providing a signal propagation delay time required for said MOS transistor; and

(b) determining a layout pattern of said MOS transistor based on said signal propagation delay time,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$(R \cdot C) / td < 1$$

where

C = the gate capacitance (F) of said MOS transistor,

R = the resistance (Ω) of a fixed potential transmission path extending from said at least one body contact to said body region,

td = signal propagation delay time (s) required for said MOS transistor, and

$td \leqq 50$ ps.

3. A semiconductor device designed by the method as recited in claim 1.

4. A semiconductor device designed by the method as recited in claim 2.

5. The semiconductor device according to claim 3,

wherein said resistance R of said fixed potential transmission path is determined by

$$R = (\rho \cdot W) / (L \cdot t_{SOI})$$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region.

6. The semiconductor device according to claim 5,

wherein said body portion includes a region extending from said body region in abutting relation with at least part of an outer periphery of said first and second semiconductor regions,

said MOS transistor further comprising

an isolation electrode formed on an insulating film formed on part of said body portion which is other than said body region and is in abutting relation with at least part of the outer periphery of said first and second semiconductor regions,

said at least one body contact including an out-of-isolation-electrode body contact formed on a region of said body portion which is opposed, as seen in plan view, to said first and second semiconductor regions, with said isolation electrode therebetween.

7. The semiconductor device according to claim 6,

wherein said body region includes a body contact definable region wherein said body contact is permitted to be formed,

wherein said gate electrode has an opening that exposes said body contact definable region, and

wherein said at least one body contact further includes an in-gate-electrode body contact formed on said body contact definable region.

8. The semiconductor device according to claim 6,

wherein said first semiconductor region includes a plurality of first semiconductor regions, and said second semiconductor region includes a plurality of

second semiconductor regions,

wherein said body portion includes a region formed between said plurality of first and second semiconductor regions so as to isolate said plurality of first and second semiconductor regions into discrete relationship, and

wherein said isolation electrode is further formed on said region of said body portion which isolates said plurality of first and second semiconductor regions into discrete relationship.

9. The semiconductor device according to claim 5,

wherein said body portion includes a region disposed in abutting relation with said first and second semiconductor regions along the gate width and extending from said body region along the gate length,

wherein said gate electrode is formed on part of said body portion which is disposed in abutting relation with said first and second semiconductor regions along the gate width, and extends further from on said body region along said gate length, and

wherein said at least one body contact includes an out-of-gate-electrode body contact formed on said region of said body portion which is opposed, as seen in plan view, to said first and second semiconductor regions, with said gate electrode therebetween.

10. The semiconductor device according to claim 9,

wherein said body region includes a body contact definable region in which said body contact is permitted to be formed,

wherein said gate electrode has an opening that exposes said body contact definable region, and

wherein said at least one body contact further includes an in-gate-electrode

body contact formed on said body contact definable region.

11. The semiconductor device according to claim 5,

wherein said at least one body contact includes:

a first body contact formed on said body portion in a position located on an outward extension line from one end of said gate electrode along the gate width, and

a second body contact formed on said body portion in a position located on an outward extension line from the other end of said gate electrode along the gate width.

12. The semiconductor device according to claim 5,

wherein said body region includes a first body region at least part of which is formed in an upper part thereof, and a second body region formed in a lower part thereof,

said second body region of the second conductivity type being of an impurity concentration higher than the impurity concentration of said first body region of the second conductivity type.

13. The semiconductor device according to claim 12,

wherein said first semiconductor region includes a first main region and a first partial semiconductor region, and said second semiconductor region includes a second main region and a second partial semiconductor region, said first and second partial semiconductor regions being formed in opposed relation in upper partial regions of said first and second semiconductor regions, said first and second partial semiconductor regions of the first conductivity type being of an impurity concentration lower than the impurity concentration of said first and second main regions of the first conductivity type,

wherein said second body region includes first and second partial body regions,

wherein said first and second partial body regions are formed under parts of said first and second partial semiconductor regions and in interface contact with said first and second main regions, respectively, said body region in other than said first and second partial body regions being defined as said first body region, and

wherein said first body region is formed out of interface contact with said first and second main regions, and said first and second partial semiconductor regions extend a predetermined distance from said first and second partial body regions toward the center of said gate electrode.

14. The semiconductor device according to claim 12,

wherein said first semiconductor region includes a first main region and a first partial semiconductor region, and said second semiconductor region includes a second main region and a second partial semiconductor region, said first and second partial semiconductor regions being formed in opposed relation in partial regions of said first and second semiconductor regions and extending vertically through said SOI layer, said first and second partial semiconductor regions of the first conductivity type being of an impurity concentration lower than the impurity concentration of said first and second main regions of the first conductivity type.

15. The semiconductor device according to claim 12,

wherein said first semiconductor region includes a first main region and a first partial semiconductor region, and said second semiconductor region includes a second main region and a second partial semiconductor region, said first and second partial semiconductor regions being formed in opposed relation in partial regions of said first and second semiconductor regions, said first and second partial semiconductor regions of

the first conductivity type being of an impurity concentration lower than the impurity concentration of said first and second main regions of the first conductivity type, and

wherein said second body region is formed in a lower central part of said body region and out of interface contact with said first and second main regions.

16. The semiconductor device according to claim 5, further comprising:

a body floating MOS transistor having an unfixed body potential,

said SOI layer including a first region having a first thickness, and a second region having a second thickness less than said first thickness,

said MOS transistor being formed on said first region,

said body floating MOS transistor being formed on said second region.

17. A computer readable recording medium which records thereon a program for embodying the method as recited in claim 1.

18. The semiconductor device according to claim 4,

wherein said resistance R of said fixed potential transmission path is determined by

$$R = (\rho \cdot W) / (L \cdot t_{SOI})$$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region.

19. The semiconductor device according to claim 18,

wherein said body portion includes a region extending from said body region in abutting relation with at least part of an outer periphery of said first and second semiconductor regions,

said MOS transistor further comprising

an isolation electrode formed on an insulating film formed on part of said body portion which is other than said body region and is in abutting relation with at least part of the outer periphery of said first and second semiconductor regions,

said at least one body contact including an out-of-isolation-electrode body contact formed on a region of said body portion which is opposed, as seen in plan view, to said first and second semiconductor regions, with said isolation electrode therebetween.

20. A computer readable recording medium which records thereon a program for embodying the method as recited in claim 2.